CLAIMS

What is claimed:

1. An apparatus, comprising

a phase frequency detector ("PFD") configured to detect a phase difference between a first signal and a second signal and configured to produce very narrow voltage pulses, said first and second signals having very high frequencies; and

a charge pump, without a feedback circuit, coupled in series with the PFD and having positive and negative current branches configured to convert the very narrow voltage pulses to current pulses for correcting the phase difference between the first and second signals.

2. The apparatus of claim 1, wherein said first and second signals being up to approximately 2 GHz in frequency.

3. The apparatus of claim 1, wherein said very narrow voltage pulses are as small as 200ps in period.

4. The apparatus of claim 1, wherein said PFD includes one or more edge triggered TSPC D flip-flops configured to have Clock to Q and Reset to Q delays of less than 100ps.

5. A charge-pump circuit, comprising:

an upper current branch configured to generate a positive current pulse, said upper current branch including a plurality of PMOS transistors;

a lower current branch to configured to generate a negative current pulse, said lower current branch including a plurality of NMOS transistors, and said lower current branch coupled to said upper branch; and

a bias circuit coupled to the upper and lower current branches with no intervening feedback circuit.

6. The charge-pump circuit of claim 5, wherein said upper current branch comprises;

first and second p-type transistors coupled together at their source terminals with a gate of the first p-type transistor coupled to receive a first voltage pulse and a gate of the second p-type transistor coupled to receive a second voltage pulse which is a logical inverse of the first voltage pulse, said first and second p-type transistors configured to steer the positive current pulse; and

third and fourth p-type transistors with their gates coupled to ground, a source of the third p-type transistor connected to a drain of the first p-type transistor and a source of the fourth p-type transistor connected to a drain of the second p-type transistor, said third and fourth p-type transistors being always on and configured to eliminate charge injection effects.

7. The charge-pump circuit of claim 6, wherein said first and second voltage pulses are as narrow as 200ps in period.

8. The charge pump circuit of claim 5, wherein said lower current branch comprises:

first and second n-type transistors coupled together at their source terminals with a gate of the first n-type transistor coupled to receive a third voltage pulse and a gate of the second n-type transistor coupled to receive a

fourth voltage pulse which is a logical inverse of the third voltage pulse, the first n-type transistor and second n-type transistors configured to steer the negative current pulse; and

third and fourth n-type transistors with their gates connected to a fifth voltage, a source of the third n-type transistor connected to a drain of the first n-type transistor and a source of the fourth n-type transistor connected to a drain of the second n-type transistor, and drains of the third and fourth n-type transistors connected to drains of the third and fourth p-type transistors in the upper current branch, said third and fourth n-type transistors being always on and configured to eliminate charge injection effects.

9. The charge-pump circuit of claim 8, wherein said third and fourth voltage pulses are as narrow as 200ps in period.

10. The charge-pump of claim 5, wherein said bias includes a positive current source connected to the upper current branch and a negative current source connected to the lower current branch, said positive and negative current sources configured to be continually on so as to provide negative and positive currents when in use.

11. The charge-pump of claim 5, further comprising a shorting buffer connected to the upper and lower current branches.

12. A high-speed PFD comprising:

a first edge-triggered asynchronous-reset TSPC D flip-flop ("TSPC DFF") with a first input coupled to receive a reference clock signal, a second input

coupled to receive a reset signal, and an output coupled to provide a first output signal;

a second TSPC DFF with a first input coupled to receive a feedback clock signal, a second input coupled to receive a reset signal, and an output to provide a second output signal; and

an OR gate with a first input coupled to receive the first output signal, a second input coupled to receive the second output signal, and a reset output coupled to provide the reset output signal for both the first and second TSPC DFFs.

13. The high-speed PFD of claim 12, wherein said first and second flip-flops are configured to produce output signals with periods as small as 100ps.

14. The high-speed PFD of claim 12, wherein said reference clock signal and said feedback clock signal being up to 2GHz in frequency.

15. The high-speed PFD of claim 10, wherein said first and second edge-triggered CMOS D flip-flops further include:

a p-precharged Domino logic gate ("p-block");

an n-precharged Domino logic gate ("n-block") coupled to the p-block; and

reset logic coupled to the n-block, said reset logic configured to perform asynchronous resetting.

16. The high-speed PFD of claim 15, wherein said p-block has no inverting clock latch.

17. The high-speed PFD of claim 15, wherein said n-block has a clock latch and wherein the reset logic is coupled to the clock latch of the n-block.

18. The high-speed PFD of claim 12, wherein the said first and second TSPC DFFs have Clock to Q and Reset to Q delays below 100ps.

19. An frequency synthesizer, comprising:

a high-speed PFD configured to detect a phase difference between a first and second signal and generate voltage pulses; and

a charge pump, without a feedback circuit, coupled in series with the high-speed PFD, and having positive and negative current branches to generate convert the voltage pulses to current pulses to correct the phase difference between the first and second signals.

20. The frequency synthesizer of claim 19, wherein said first and second signals being up to approximately a 2 GHz in frequency.

21. The frequency synthesizer of claim 19, wherein said high-speed PFD includes one or more fast edge-triggered TSPC D flip-flops configured to generate voltage pulses with a period as small as 200ps and Clock to Q and Reset to Q delays smaller than 100ps.